IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A demodulator circuit for emulating the down conversion of an input signal x(t) with a local oscillator (LO) signal, said demodulator circuit comprising:

a first mixer for receiving said input signal x(t), and mixing said input signal x(t) with a multi-tonal mixing signal $\varphi 1$, to generate an output signal $\varphi 1$ x(t);

a second mixer for receiving said signal $\varphi 1$ x(t) as an input, and mixing said signal $\varphi 1$ x(t) with a mono-tonal mixing signal $\varphi 2$, to generate an output signal $\varphi 1$ $\varphi 2$ (t);

a first signal generator for generating an oscillator signal f1;

a second signal generator for generating said mono-tonal mixing signal $\varphi 2$, where the frequency of f1 is a multiple of the frequency of $\varphi 2$; and

a logic circuit for receiving said oscillator signal f1 and said mono-tonal mixing signal $\varphi 2$, and generating said multi-tonal mixing signal $\varphi 1$, where $\varphi 1 * \varphi 2$ has significant power at the frequency of said local oscillator signal being emulated, neither of said $\varphi 1$ nor said $\varphi 2$ having significant power at the carrier frequency of said input signal x(t) or said LO signal being emulated.

Claim 2 (Original): The circuit of claim 1 wherein said logic circuit comprises an exclusive OR gate (XOR), and $\varphi 1$ = f1 XOR $\varphi 2$.

Claim 3 (Original): The-circuit of claim 1 wherein unwanted power at baseband is minimized by adjusting the frequency of said $\varphi 2$ signal such that unwanted RF tones do not fall on top of said input signal x(t) at baseband.

Claim 4 (Original): The circuit of claim 1 wherein unwanted power at baseband is minimized by frequency hopping said φ2 signal so that the probability of unwanted RF tones falling on top of φ1 * φ2 x(t) insignificantly reduced.

Claim 5 (Original): The circuit of claim 1 wherein said first signal generator comprises:

an oscillator for-generating an oscillator signal; and

a regenerative divider for receiving said oscillator signal and converting said oscillator signal to said f1 signal.

Claim 6 (Original): The circuit of claim 5 wherein said oscillator is a voltage-controlled oscillator.

Claim 7 (Original): The circuit of claim 5 wherein said oscillator that is tuned to a multiple of the carrier frequency of said input signal x(t) and said regenerative divider comprises a divide-by-n element.

Claim 8 (Original): The circuit of claim 6 wherein said oscillator further comprises a high pass filter.

Claim 9 (Original): The circuit of claim 1 wherein said first signal generator comprises an oscillator that is tuned to a divisor of the carrier frequency of said input signal x(t) and a multiply-by-n element.

Claim 10 (Original): The circuit of claim 1 wherein said second signal generator comprises:

a frequency controller; and

a square wave generator.

Claim 11 (Original): The circuit of claim 10 wherein said second signal generator further comprises:

a divide-by-2 element to ensure that a fifty percent duty cycle is provided.

Claim 12 (Original): The circuit of claim 10 wherein said frequency controller is operable to hop said $\varphi 2$ signal from one frequency to another, reducing the probability of the output of said circuit having power at an unwanted frequency.

Claim 13 (Original): The circuit of claim 10 wherein said frequency controller is responsive to noise in said output signal $\varphi 1\ \varphi 2\ x(t)$ by adjusting the frequency of $\varphi 2$.

Claim 14 (Original): The circuit of claim 10 wherein said first mixer comprises an active mixer.

Claim 15 (Original): The circuit of claim 14 wherein said first mixer comprises an active mixer having adjustable performance.

Claim 16 (Original): The circuit of claim 15, wherein said active mixer has adjustable gain.

Claim 17 (Original): The circuit of claim 15, wherein said active mixer has adjustable linearity.

Claim 18 (Original): The circuit of claim 15, wherein said active mixer comprises a current-source whose parameters can be adjusted to control gain and linearity of said active mixer.

Claim 19 (Original): The circuit of claim 15, wherein said active mixer comprises multiple driver components, each for receiving a different input signal in a multi-standard radio.

Claim 20 (Original): The circuit of claim 14 further comprising a high pass filter electrically connected between said first mixer and said second mixer.

Claim 21 (Original): The circuit of claim 20 wherein said second mixer comprises a passive mixer.

Claim 22 (Original): The circuit of claim 21, wherein each of said active mixer, said high pass filter and said passive mixer is a differential device.

Claim 23 (Original): The circuit of claim 22, wherein said high pass filter comprises a resistor dividing network for setting the common mode voltage output.

Claim 24 (Original): The circuit of claim 5 wherein said oscillator, said regenerative divider and said logic circuit are differential.

Claim 25 (Original): The circuit of claim 24 wherein said logic circuit comprises two exclusive OR (XOR) gates.

Claim 26 (Original): The circuit of claim 24 wherein said logic circuit comprises two exclusive-NOR (XNOR) gates.

Claim 27 (Original): The circuit of claim 24 wherein said logic circuit comprises four AND gates and two OR gates arranged to generate:

$\varphi 1P = (\varphi 2P \text{ AND } f1P) \text{ OR } (\varphi 2N \text{ AND } f1N)$; and

$\varphi 1N = (\varphi 2P \text{ AND } f1N) \text{ OR } (\varphi 2N \text{ AND } f1P)$.

Claim 28 (Original): The circuit of claim 24 wherein said logic circuit comprises four semiconductor switches arranged to generate:

$\varphi 1P = (\varphi 2P \text{ AND } f1P) \text{ OR } (\varphi 2N \text{ AND } f1N)$; and

$\varphi 1N = (\varphi 2P \text{ AND } f1N) \text{ OR } (\varphi 2N \text{ AND } f1P)$.

Claim 29 (Original): A method of emulating the demodulation of an input signal x(t) to the product of said input signal with a local oscillator (LO) signal, said method comprising the steps of:

generating an oscillator signal f1;

generating a mixing signal $\varphi 2$, where f1 is four times the frequency of $\varphi 2$;

generating an aperiodic mixing signal $\varphi 1$, using a logic circuit which receives said oscillator signal f1 and said second mixing signal $\varphi 2$, as inputs, where $\varphi 1^* \varphi 2$ has significant power at the frequency of a local oscillator signal being emulated, and neither of said $\varphi 1$ nor

said $\varphi 2$ having significant power at the frequency of said input signal x(t), said LO signal being emulated, or said output signal $\varphi 1$ $\varphi 2$ x(t);

mixing said input signal x(t) with said aperiodic mixing signal $\varphi 1$, to generate an output signal $\varphi 1$ x(t); and

mixing said signal $\varphi 1$ x(t) with a second mixing signal $\varphi 2$, to generate an output signal $\varphi 1$, $\varphi 2$ x(t).

Claim 30-31 (Canceled).